AN4616

Driving Microchip SiC MOSFETs

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PURPOSE

This application note provides design guidance for properly selecting gate-source voltages for Microchip's SiC MOSFET products, along with related device performance and behavior.

This note applies to Microchip part numbers of the type MSCXXXSMAXXX.

SPECIFYING GATE DRIVE VOLTAGES FOR SIC MOSFETS

The way gate drive voltages are specified on data sheets varies by manufacturer, but most will have some form of Table 1. We begin by defining some terms:

- V_{GS} is the applied voltage between the MOSFET's gate and source terminals.
- V_{GSon} is the steady-state V_{GS} applied to turn the MOSFET on.
- V_{GSoff} is the steady-state V_{GS} applied to turn the MOSFET off.
- V_{GSmax} is the manufacturer's maximum allowed steady-state V_{GS}, shown for both negative and positive extremes.
- $V_{GS,OP}$ is the manufacturer's recommended steady state values for V_{GSon} and V_{GSoff}.

Some data sheets do not specify V_{GSon} and V_{GSoff}; similar to silicon MOSFETs, different applications may call for different optimal values.

MICROCHIP RECOMMENDATIONS

For optimal device performance and system stability, Microchip SiC MOSFETs are best driven using V_{GSon} = +20V and V_{GSoff} = -5V. Microchip SiC MOSFETs still perform well at lower absolute values of V_{GSon} and V_{GSoff}, but as with any design, the additional losses associated with sub-optimal drive conditions should be analyzed and understood. To this end, the reasoning behind optimal V_{GSon} and V_{GSoff} are different, and the expected trade-offs for each case are described in the following sections.

ON STATE GATE DRIVE VOLTAGE, V_{GSon}

Driving Microchip SiC MOSFETs with a lower V_{GSon} will exhibit:

- Increased on-state resistance, resulting in higher conduction loss
- Reduced peak (saturation) current capability
- Longer short circuit withstand time
- Extended gate oxide lifetime
- Increased switching loss under the same gate resistance.

On State Resistance, R_{DSon}

The four curves in Figure 1 show how the normalized R_{DSon} (normalized to R_{DSon} at 25°C and 20V gate voltage) increases with junction temperature, T_j. Data is shown for Microchip's largest SiC MOSFET die at each of four voltage classes: 700V, 15 mΩ; 1200V, 17 mΩ; 1700V, 35 mΩ; and 3300V, 25 mΩ.

Some general observations include:

- The increase of R_{DSon} for SiC MOSFETs with temperature is much lower than that of silicon MOSFETs.
- Microchip SiC MOSFETs show a lower increase of R_{DSon} at elevated T_j than other SiC MOSFET suppliers.
- At V_{GSon} = 18V, R_{DSon} shows a minor shift which gets even smaller at higher T_j.
- At V_{GSon} = 15V, the increase of R_{DSon} is more substantial, particularly at lower T_j.

TABLE 1: GATE SOURCE VOLTAGE SPECIFICATION

Characteristics	Symbol	Conditions	Value	Unit
Gate-Source Voltage	V_{GSmax}	Absolute maximum DC values	-10 to 23	V
	$V_{GS,OP}$	Recommended DC operating values	-5 to 20	V

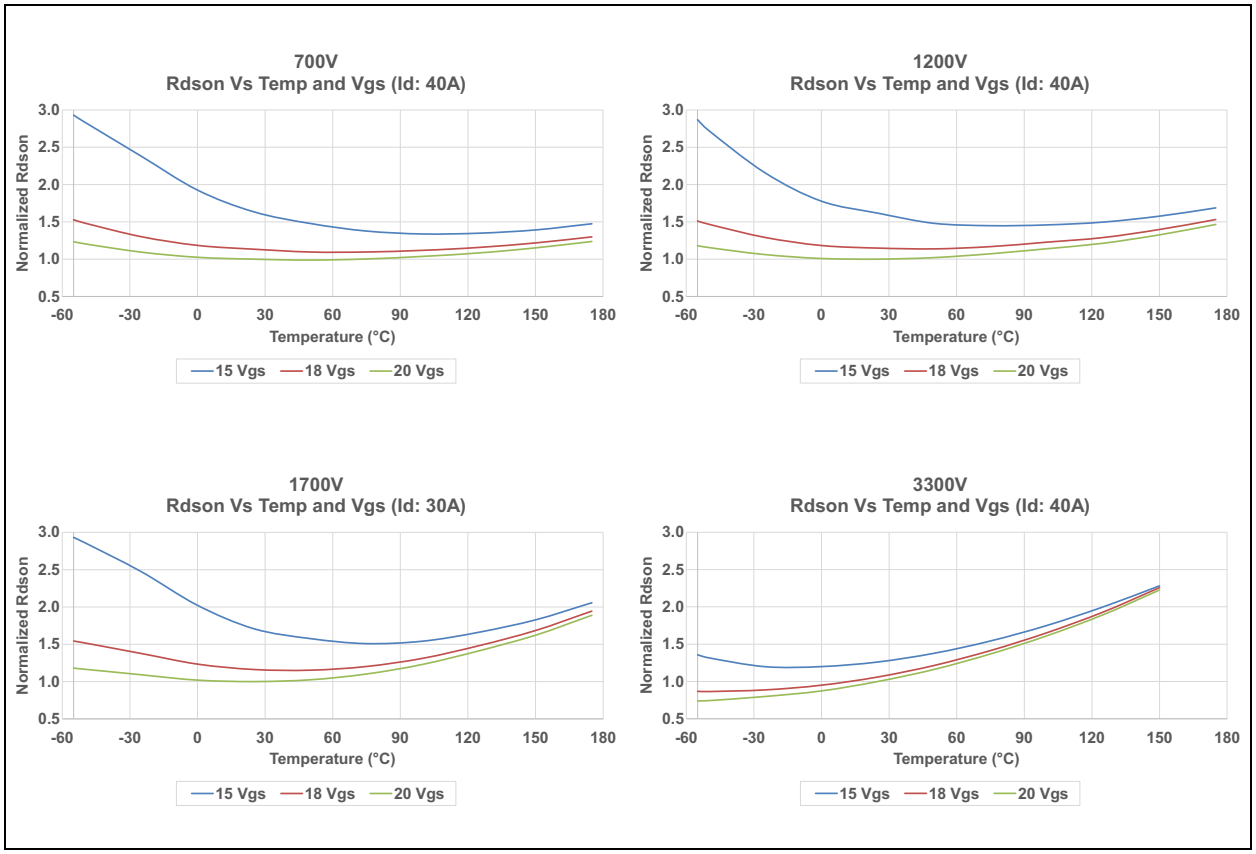

FIGURE 1: *Temperature Dependency of R_{DSon} Under Different Gate Voltage of Different Voltage Families.*

Designing for V_{GSon} < 20V

Due to SiC's wide band gap, a higher electric field is required to invert the semiconductor of a MOS-gated transistor than is required for silicon. The electric field can be increased either by raising the applied V_{GSon} or by reducing the thickness of the gate oxide. Raising V_{GSon} may call for a new gate driver design, while reducing the oxide thickness could make the device more susceptible to failure. A third way to get more current is to increase die size, but this increases cost. Clearly the best technical and commercial choice is a new gate driver design, but what compromises are made if the ideal V_{GSon} = 20V is impossible to achieve?

EFFECT ON R_{DSon}

When driving at lower values of V_{GSon}, designers should analyze how R_{DSon} changes across the junction temperature range of interest. If the R_{DSon} across relevant T_j is consistently within a close range of the R_{DSon} at V_{GSon} = 20V, the final design can accommodate these small differences and be extremely robust. For Microchip SiC MOSFETs, production measurement of R_{DSon} shows V_{GSon} = 20V is an excellent predictor of R_{DSon} at V_{GSon} = 18V; in the case of a 1200V SiC MOSFET at T_j = 175°C, R_{DSon} at V_{GS} = 18V is only 4% higher than R_{DSon} at V_{GS} = 20V.

In contrast, the comparison of R_{DSon} at V_{GSon} = 20V and V_{GSon} = 15V requires careful consideration. The variance is approximately 4x higher for V_{GSon} = 15V and dependent upon device threshold voltage, $V_{GS(th)}$. For this reason, Microchip does not recommend driving SiC MOSFETs of type MSCXXXSMAXXX at V_{GSon} = 15V. If they must be driven with 15V, a sufficient design margin for R_{DSon} should be considered. Contact your local Microchip sales office for support.

PARALLEL-CONNECTED SIC MOSFETS

There is a final point to be made about parallel-connected SiC MOSFETs and V_{GSon} < 20V. One can observe from the charts that the temperature coefficient of R_{DSon} may not be positive across the entire range of relevant T_j. In an extreme example, consider the 700V SiC MOSFET at V_{GSon} = 15V. This gate drive situation results in a SiC MOSFET with a negative temperature coefficient up to T_j = 80-100°C. Ensuring that paralleled devices will evenly share current is a risk against which the design should be safeguarded. However, much as in the previous paragraphs, using V_{GSon} = 18V is the simplest solution and is well-suited for most applications.

PEAK CURRENT CAPABILITY

When driving with a lower V_{GSon}, the MOSFET channel is not fully enhanced, and the maximum current is reduced.

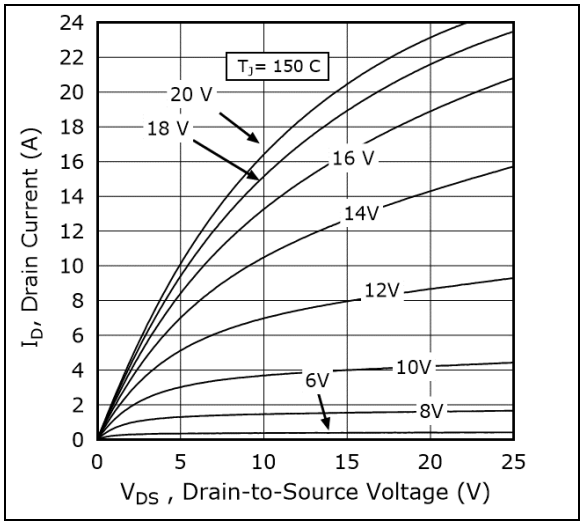

FIGURE 2: *I-V Curve of MSC360SMA120B Under Different Driving Voltages at T_j = 150°C.*

Figure 2 shows the I-V curve of MSC360SMA120B under different driving voltages at T_j = 150°C. Note the small separation between the R_{DSon} curves at V_{GSon} = 20V and V_{GSon} = 18V, and compare this to the bigger differences in R_{DSon} as V_{GSon} drops increasingly below 16V. Some important considerations include:

- An over-current protection scheme based upon the maximum current may fail to trigger. Designers should account for the higher variability of R_{DSon} at lower V_{GSon}.
- The small-signal transconductance, gm, is higher at lower V_{GSon}. This effect can lead to switching instability, since V_{GS} may be in a middle range in the presence of high drain-source voltage – resulting in a short circuit event. (The peak short circuit current will be governed by the precise value and duration of V_{GSon}. See the next subsection.)

SHORT CIRCUIT WITHSTAND TIME

When driving with lower V_{GSon}, the maximum current will be lower under short circuit conditions, which can lead to a longer short circuit withstand time.

The following plot shows the short circuit withstand time (SCWT) in relation to gate and drain voltage for MSC035SMA070B measured with V_{DS} = 350V, 470V and 560V and V_{GSon} = 20V, 18V and 15V. It can be seen that the drain voltage is the most significant factor affecting SCWT, followed by V_{GS}.

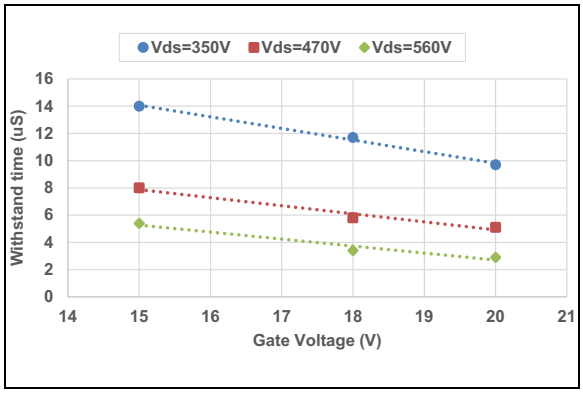

FIGURE 3: *Short Circuit Withstand Time of MSC035SMA070B.*

In applications where short circuits may occur, the following considerations should be made:

- The SCWT specified in the data sheet is the typical time to failure, as defined by the device no longer exhibiting proper electrical function. In reality, the failure occurs after the device is switched off, when the latent heat generated causes irreversible damage. In essence, the delay does not happen when the measurement says it happens. Because of this delay, data sheet's SCWT can only be seen as a typical number.
- A more reasonable requirement would be that a specified number of devices are still operational after a specified number of short circuit events.
- Short circuit withstand time can be extended by increasing the device size or using multiple devices designed to drive at a reduced current level with source degeneration.

For additional guidance and insight, please contact your local Microchip sales team.

Projected Lifetime

The below graph indicates that for every 2.5V increase in V_{GSon}, the projected lifetime of the gate oxide is reduced by an order of magnitude. This relationship applies over a wide range. It is a wear out mechanism due to accumulated damage over time.

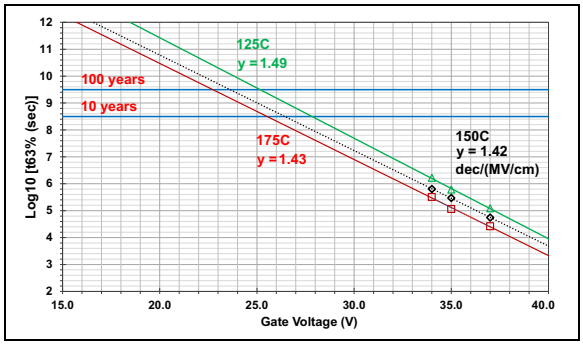

FIGURE 4: *Projected Device Lifetime Under Different Gate Voltage.*

The lifetime of the gate oxide is mostly determined by the steady state gate ON drive voltage. The +23V maximum rating on the gate is a recommendation for steady state gate voltage based on the projected lifetime of the device. Transient overshoots in V_{GSon} do not materially affect the device lifetime because of their brief duration. As an example, assume a rectangular overshoot for 20 ns at 25V with a nominal gate voltage of 20V. Per the oxide lifetime graph, the rate of degradation of the oxide during the pulse is 80 times higher. However, with a switching frequency of 100 kHz, the duty factor is 20/100,000 = 0.002. The relative stress, then, is only 80 × 0.002 = 16%.

It should be noted that transient V_{GS} is not observable at the package pins. The gate and source lead inductances make it difficult to measure the actual gate voltage overshoot. Due to the high capacitance of the gate, the gate drive is normally over-dampened, and overshoot is rarely a problem. This is easiest to determine in simulations.

Summary of V_{GSon}

Microchip SiC MOSFETs can operate at +18V drive voltage with little loss in performance compared with the recommended +20V drive voltage. As can be seen in the above graphs, the increase in R_{DSon} is much larger at 25°C than at 100°C-150°C. A system generally is penalized less by conduction loss than would be implied by the difference at 25°C if the die is hot. While the switching losses may be slightly higher under the same gate resistance, and saturation current will be lower, the positive trade-off is a longer short circuit withstand time.

Operation at V_{GSon} < 18V gate drive comes with elements of risk and should only be used if there is sufficient margin in R_{DSon}. Current sharing between paralleled devices can be problematic at colder junction temperatures. If V_{GSon} < 18V is needed, please contact your Microchip team for design support.

OFF STATE DRIVING VOLTAGE, V_{GSoff}

Microchip SiC MOSFETs are normally OFF power transistors. **A negative V_{GSoff} is not required to keep the switch OFF during steady state. Rather, it is used to minimize switching loss and enhance switching stability.**

- The presence of source inductance can slow the device turn-off process. A negative V_{GSoff} is used to overcome this effect.
- A negative V_{GSoff} provides more margin to avoid false turn on (also called shoot-through or cross conduction) during switching transients.
- A negative V_{GSoff} has been used for decades with silicon IGBTs. Negative gate drive is not unique to SiC.
- More complex modules with distributed transistors need a higher (more negative) V_{GSoff} to avoid instability. Single transistor discrete designs can get by with very little negative V_{GSoff}.

Third Quadrant Conduction Performance

Unlike a silicon IGBT, SiC MOSFETs can conduct current in both directions. The figure below shows the so-called “third quadrant” performance of Microchip’s MSC360SMA120B; simply put, this is the drain current when the drain voltage is reversed. The body diode carries reverse drain current if the MOSFET’s channel is turned OFF. In the case of V_{GSoff} = -5V, all current flows through the body diode. As V_{GS} is increased, the channel begins to form but maintains a substantial voltage drop even at V_{GS} = 0V, meaning the body diode still carries most of the reverse current. Following the switching transient, the channel can be turned ON to also conduct the reverse current to further improve conduction losses in a technique known as synchronous rectification.

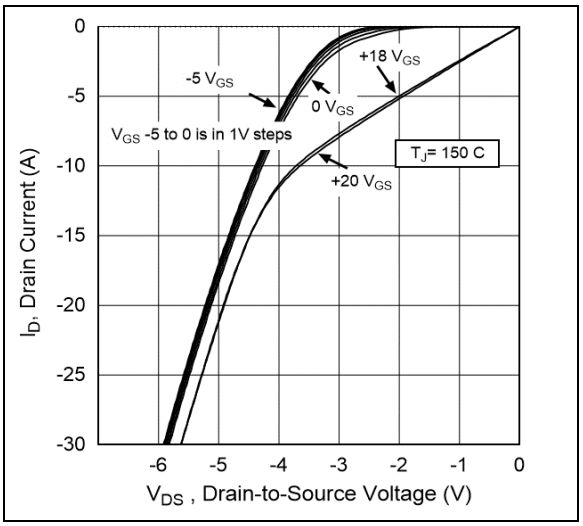

FIGURE 5: *Third Quadrant I-V Curve of MSC360SMA120B.*

BODY DIODE ROBUSTNESS

There are no restrictions on use of the body diode in Microchip’s SiC MOSFETs, but this is not true for all SiC MOSFET suppliers. Recent third-party measurements have shown that competitors’ devices demonstrate body diode degradation to varying severity – in some cases, conduction losses increase by 20% after 168 hours; while in others, conduction losses more than double in less than 10 hours[1]. The degradation mechanism is called recombination-enhanced dislocation motion; the phenomena is well understood and has been observed in other semiconductors, such as SiGe, CdS, and GaAs. With certain device knowhow, the effects can be mitigated in SiC.

Again, **it should be emphasized that customers can use Microchip's SiC MOSFET body diodes with confidence**, but should you have any questions, please contact your local Microchip sales office.

Switching Noise Immunity

There are important precautions to consider if using V_{GSoff} = 0V for SiC MOSFETs in high-speed, hard switching applications. Before diving into these precautions, some discussion about threshold voltage and pinch-off voltage is warranted.

Table 2 is from the data sheet of Microchip's 1200V, 80 mΩ SiC MOSFET in TO-247 package. Due to industry convention, the nominal threshold voltage V_{th} is measured under the conditions of V_{GS} = V_{DS}, T_j = 25°C, and a drain current of only 1 mA. Since the drain current associated with V_{th} is so low, the more relevant parameter to use for designs is known as the pinch-off voltage, V_p. The pinch-off voltage V_p is the value of V_{GS} that produces a given drain current at a specific V_{DS}.

Accordingly, the value of V_p has a dependence on VDS that varies by MOSFET architecture. Trench MOSFETs have a much higher variation in V_p than planar MOSFETs; for this reason, to help ensure safe operation, trench MOSFETs are designed such that V_{th} at 25°C is higher than needed. This means that planar MOSFETs offer greater design margin around V_p, which brings us at last to the key message on switching noise immunity.

The "real" margin for switching noise immunity should be set by V_p at the highest possible V_{DS} and the maximum allowed T_j. For our current generation SiC MOSFETs, Microchip guarantees turn-off with V_{GS} = 0V at T_j = 175°C. Using a negative V_{GSoff} provides more margin on V_p, which enhances switching stability and is the most certain way to prevent false turn-on.

The false turn-on in a half bridge configuration is commonly induced by the miller capacitance (drain to gate capacitance C_{GD}) as shown in Figure 6. When top device Q2 is turned ON the high midpoint (phase leg output) dV/dt will induce current flow through C_{GD} that creates a voltage difference across gate resistor R_{OFF}. This voltage difference will make the actual gate voltage V_{GS} on bottom device Q1 higher than steady state OFF voltage V_{EE}. This voltage can be high enough to turn Q1 ON, the margin on V_p prevent this false turn-on.

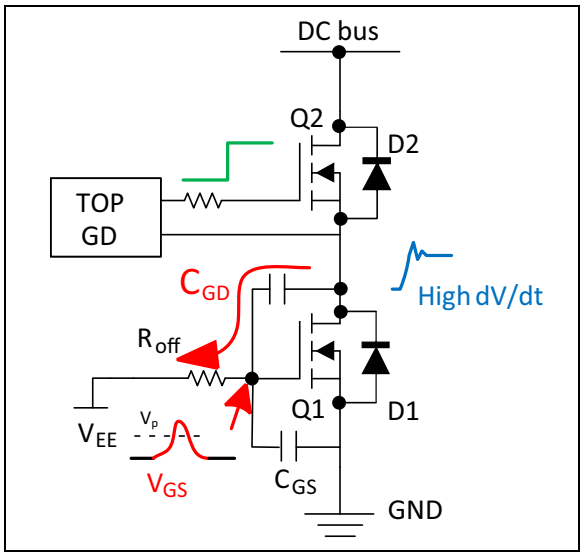

FIGURE 6: *Switching Induced False Turn ON in a Half Bridge Configuration.*

Summary of V_{GSoff}

Due to the previous discussion, Microchip does not recommend the use of V_{GSoff} = 0V. For single-ended topologies with no danger of shoot-though (e.g., flyback, buck, or boost topologies), it is possible to use V_{GSoff} = 0V. Should V_{GSoff} = 0V be absolutely required, attention should be given to proper gate-source loop design. Specifically, designers should try to minimize three things: (i) parasitic drain-gate capacitance, (ii) gate-source loop inductance, and (iii) shared inductance between the gate-source loop and main current commutation loop.

TABLE 2: GATE-SOURCE THRESHOLD VOLTAGE OF MSC080SMA120B

Symbol	Characteristics	Test Conditions	Minimum	Typical	Maximum	Unit
$V_{GS(th),25°C}$	Gate-source threshold voltage at 25°C	V_{GS} = V_{DS}, Io = 1 mA, T_j = 25°C	1.8	2.8	—	V

KEY TAKEAWAYS

This application note provides guidance on Microchip SiC MOSFET gate-source voltage specifications and design considerations for making the most effective gate driver circuit. The following are key takeaways.

1. For the best possible switching and conduction performance, Microchip recommends driving with V_{GSon} = +20V and V_{GSoff} = -5V.
2. It is permissible to deviate from these recommendations. Microchip SiC MOSFETs can operate at +18V with slight reductions in current capability and turn-on efficiency, but comes with the benefit of longer short circuit withstand time.
3. Driving current-generation Microchip SiC MOSFETs using V_{GSon} = 15V is not recommended. If this situation cannot be avoided, please contact Microchip for design assistance.
4. Microchip guarantees turn-off with V_{GS} = 0V at T_j = 175°C. That said, using a negative V_{GSoff} provides greater margin around V_p, which enhances switching stability and is the most certain way to prevent false turn-on.

REFERENCE

1. M. Kang *et al.*, “Body Diode Reliability of Commercial SiC Power MOSFETs”, *2019 IEEE 7th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2019, pp. 416-419.

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